Q.1 Compare bipolar jxn transistor with field effect transistor. what is basic mos transistor?

Ans:

FET	BJT.
① FET is an unipolar SC device because its operation depends upon the flow of majority carrier. i.e either holes or electrons.	① BJT is a bipolar sc device. because the current constituting elements are both majority carriers as well as minority carriers.
② FET is a voltage controlled device	② BJT is a current controlled device.
③ FET is less noisy. Because there are no jxn.	③ BJT is much noisy than FET.
④ Higher frequency Response	④ frequency variation affects the performance.
⑤ Good thermal Stability because of absense of carrier	⑤ Temperature dependent thermal runway may cause.
⑦ Costlier than BJT	Relatively Cheaper.
⑧ Small sized	Comparatively bigger.

Q.1 Draw and explain various steps involved in n-well CMOS fabrication.

Ans: The n-well process is quite often used for CMOS fabrication. The n-well process has advantages over p-well process.

These are (i) the substrate bias has lesser effect on transistor threshold vltg.

(ii) parasitic capacitance associated with source and drain region is very low. The fabrication steps for n-mos is defined in the fig.

formation of n-well regions

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Define nmos and pmos active area.

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field and gate oxidation (thinox.)

↓

form and pattern polysilicon.

↓

p^+ diffusion & n^+ diffusion

↓

Contact cuts.

↓

↓

deposit and pattern metallization

↓

over glass with cuts for bonding pads.

① The structure of p-type substrate in which n-device are formed by suitable masking and diffusion.

② The diffusion step should be made with extra precaution of the threshold vltg. and breakdown vltg of the transistors is affected by n-well doping concentration and depth of n-well

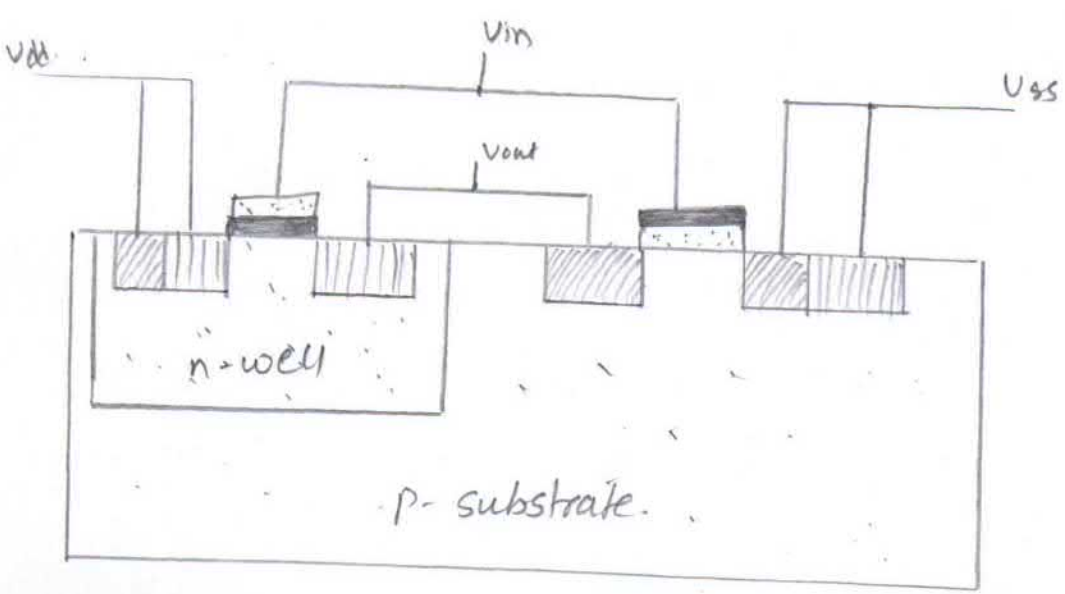


fig. CMOS n-well inverter

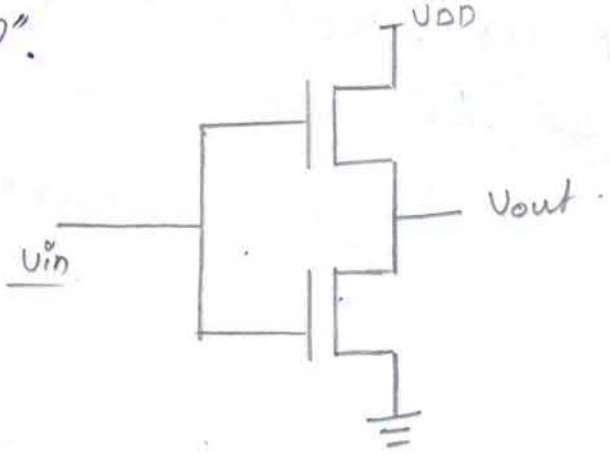
Q.2. Discuss the short circuit power dissipation in a CMOS ckt. Derive the expression for total power dissipation.

Ans :- There are two components that establish the amount of power dissipated in CMOS circuit these are.

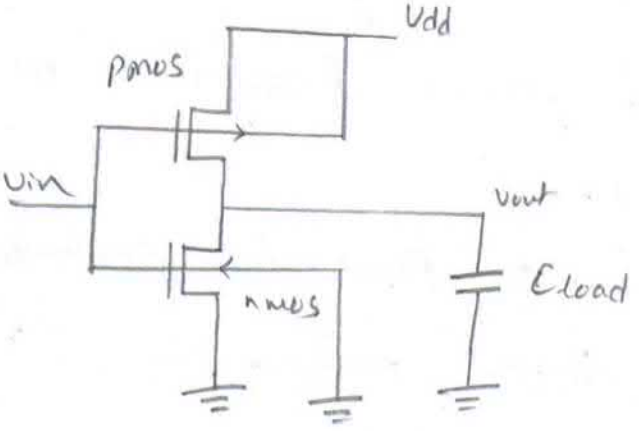
① Static Dissipation :- Due to leakage current or current drawn continously from the power supply.

② Dynamic Dissipation :- Due to the switching transit current or charging and discharging of load capacitance.

① Static Dissipation :- Consider a complement CMOS gate as shown in fig. If the I/P=0 the associated n-device is off and p-device is "ON" the output vltg is V_{DD} or logic 1 when the O/P is 1 the associated n device is ∅ biased "ON".



(iii) Dynamic Dissipation :- During switching events where the o/p load capacitance is alternatingly charged up and charged down the cmos inverter inevitably dissipates power.



Assuming periodic I/P & o/p waveforms the average power dissipated by any device over one period can be found as follow.

$$P_{avg} = \frac{1}{T}\int_0^T v(t)\cdot i(t)\,dt.$$

$$P_{avg} = \frac{1}{T}\left[\int_0^{T/2} V_{out}\left(-C_{load}\frac{dV_{out}}{dt}\right)dt + \int_{T/2}^{T}(V_{dd}-V_{out})\left(C_{load}\frac{dV_{out}}{dt}\right)dt\right]$$

Evaluate the Integrals.

$$P_{avg} = \frac{1}{T} C_{load} V_{DD}^2.$$

Noting that $f = 1/T$ this expression can also be written as.

$$P_{avg.} = C_{load} \cdot V_{DD}^2 \cdot f.$$

Q. 2 Define noise margin. The Expression for V_{OH}, V_{IL}, V_{OL}, V_{IH} for depletion load n-MOS inverter.?

Ans Noise margin :- is the ratio by which the signal exceeds the min. acceptable amount. It is normally measured in decibels.

We will consider the critical Vltg. points V_{OH}, V_{OL}, V_{IL} and V_{IH} for this inverter circuit.

Calculation of V_{OH} :- when the I/P vltg. Vin is smaller than driver threshold vltg. V_{TO}. the driver transistor is turned off and does not conduct any drain current.

$$I_{D\,load} = \frac{K_{a\,load}}{2}\left[2\left[V_{T\,load}(V_{OH})\right]\cdot(V_{DD}-V_{OH}) - (V_{DD}-V_{OH})^2\right] = 0$$

The only valid solution in linear region is $V_{OH} = V_{DD}$.

Calculation of V_{OL} :- To calculate the o/p low vltg V_{OL}, we assume that the I/P vltg Vin of the inverter is equal to $V_{OH} = V_{DD}$.

$$V_{OL} = V_{OH} - V_{TO} - \sqrt{(V_{OH}-V_{TO})^2 - \left(\frac{K_{load}}{K_{driver}}\right)\cdot\left(V_{Tload}\cdot(V_{OL})\right)^2}$$

Calculation for V_{IL}:- By definition the slop of the VTC is equal to (-1) i.e. $\frac{dV_{out}}{dV_{in}} = -1$ when the o/p vltg is $V_{IL} = V_L$.

$$V_{IL} = V_{TO} + \left(\frac{K_{load}}{K_{driver}}\right)\cdot\left[V_{out} - V_{DD} + \left|V_{Tload}(V_{out})\right|\right]$$

Calculation for V_{IH}:- V_{IH} is larger of the two vltg points on the VTC at which the slope is equal to (-1). Since the o/p vltg corresponding to this operating point is relatively small.

$$V_{IH} = V_{TO} + 2V_{out} + \left(\frac{K_{load}}{K_{driver}}\right) + \left[-V_{Tload}(V_{out})\right]\cdot\left(\frac{dV_{Tload}}{dV_{out}}\right)$$

$$\frac{dV_{Tload}}{dV_{out}} = \frac{\gamma}{2\sqrt{|2\phi_f| + V_{out}}}$$